

ESL to RTL Verification Progressive Refinement and Reuse Paradigm

TSMC Open Innovation Platform

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TSMC

Agenda

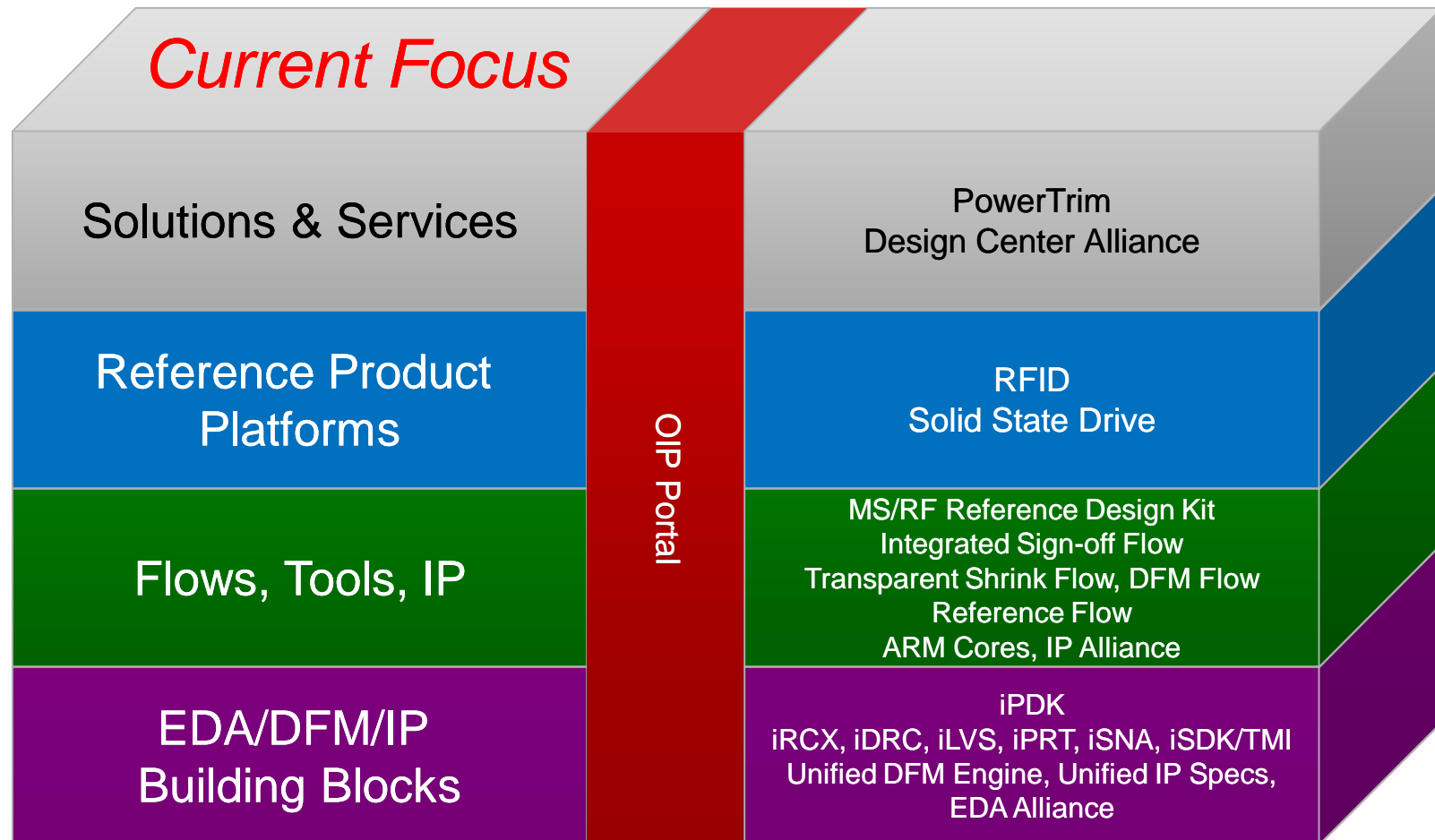
- TSMC Open Innovation Platform (OIP) and ESL Enablement
- Design Verification Challenges
- ESL to RTL Verification
 - Reuse ESL models for RTL Verification
 - Reuse ESL Testbench for RTL Verification
 - Unified Functional Coverage from ESL to RTL
 - Unified Debug from ESL to RTL



TSMC Property

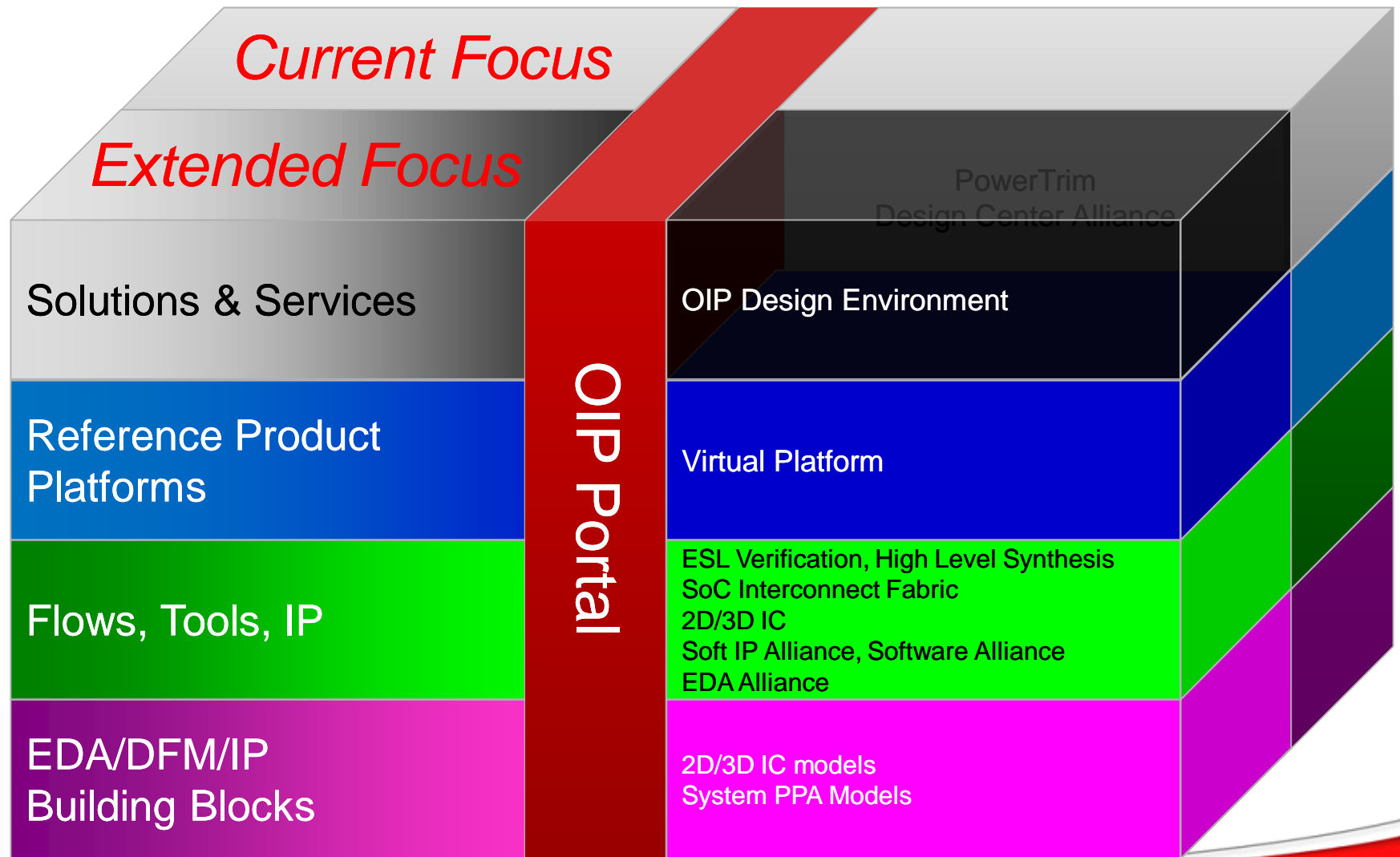
Open Innovation Platform

Current Focus - Enable More than Moore



Open Innovation Platform

Extended Focus - Enable More than Moore



TSMC Open Innovation Platform (OIP) ESL Enablement Flow



- A collaboration model to enable mutual customers to successfully reach production goals at 40nm and below.

- The entire design and verification ecosystem must move above RTL to make designs viable below 40nm

- TSMC Open Innovation Platform (OIP) collaborates with EDA partners to enable the entire ESL ecosystem
 - ESL Verification (ESL to RTL Reuse methodology)
 - ESL Virtual Prototyping and PPA
 - ◆ Early Power, Performance and Area development
 - ◆ Early Software Development
 - ESL Design (High Level Synthesis)

Design Verification Challenges and ESL

- Functional Design Verification Challenges
 - Design Verification (DV) is now the long pole to design tape-out.
 - 50 to 70% of project resources go to DV.
 - ◆ *Comprehensive Functional Verification: The Complete Industry Cycle* by Bruce Wile, John Goss, Wolfgang Roesner
 - More than 60% of designs require re-spin due to functional bugs.
 - ◆ *John Blyler, Editorial Director of Extension Media, Chip Design.*

- How does ESL Verification help ?
 - Faster Development
 - ◆ ESL abstraction levels reduce Testbench development time.

 - Faster Simulation
 - ◆ ESL testbench + design simulates orders of magnitude faster than RTL.

 - Faster Debug
 - ◆ Debug at ESL/TLM is lot easier than debug at cycle accurate RTL

 - Earlier Verification
 - ◆ Find bugs *before* committing to RTL.

 - Faster Time to Production because of faster Develop->Simulate->Debug Loop

Why ESL to RTL Verification Reuse Methodology ?

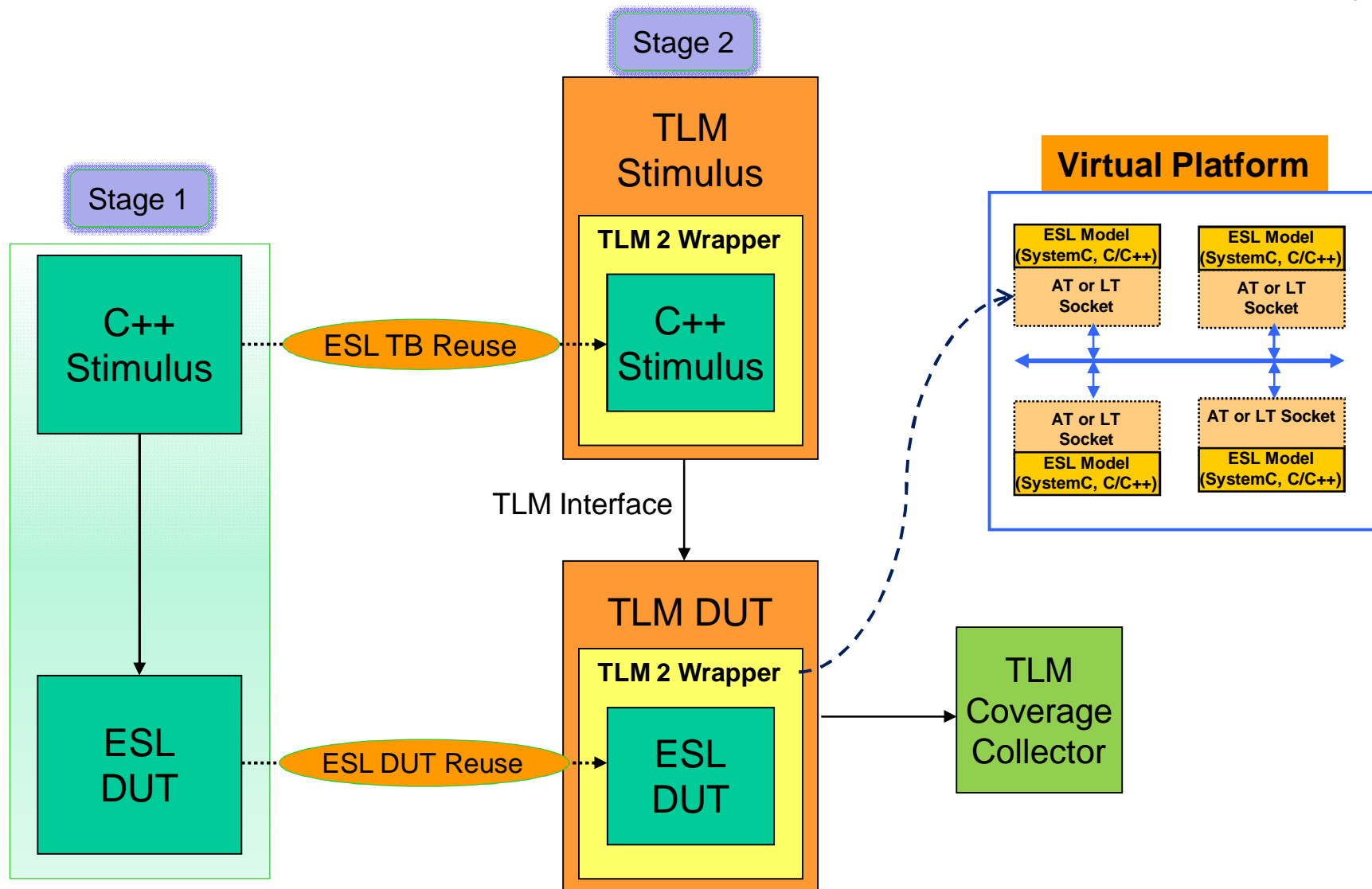
- You cannot completely verify at ESL
 - RTL Verification is still required before gates, tape-out, silicon.
 - ESL Verification with TLM 2.0 LT/AT models does not account for clock level concurrency

- You create more than twice as much work without reuse
 - Without Reuse of ESL Testbench/Environment, you will simply reinvent the wheel at RTL Level with it's longer time to develop, simulate and debug

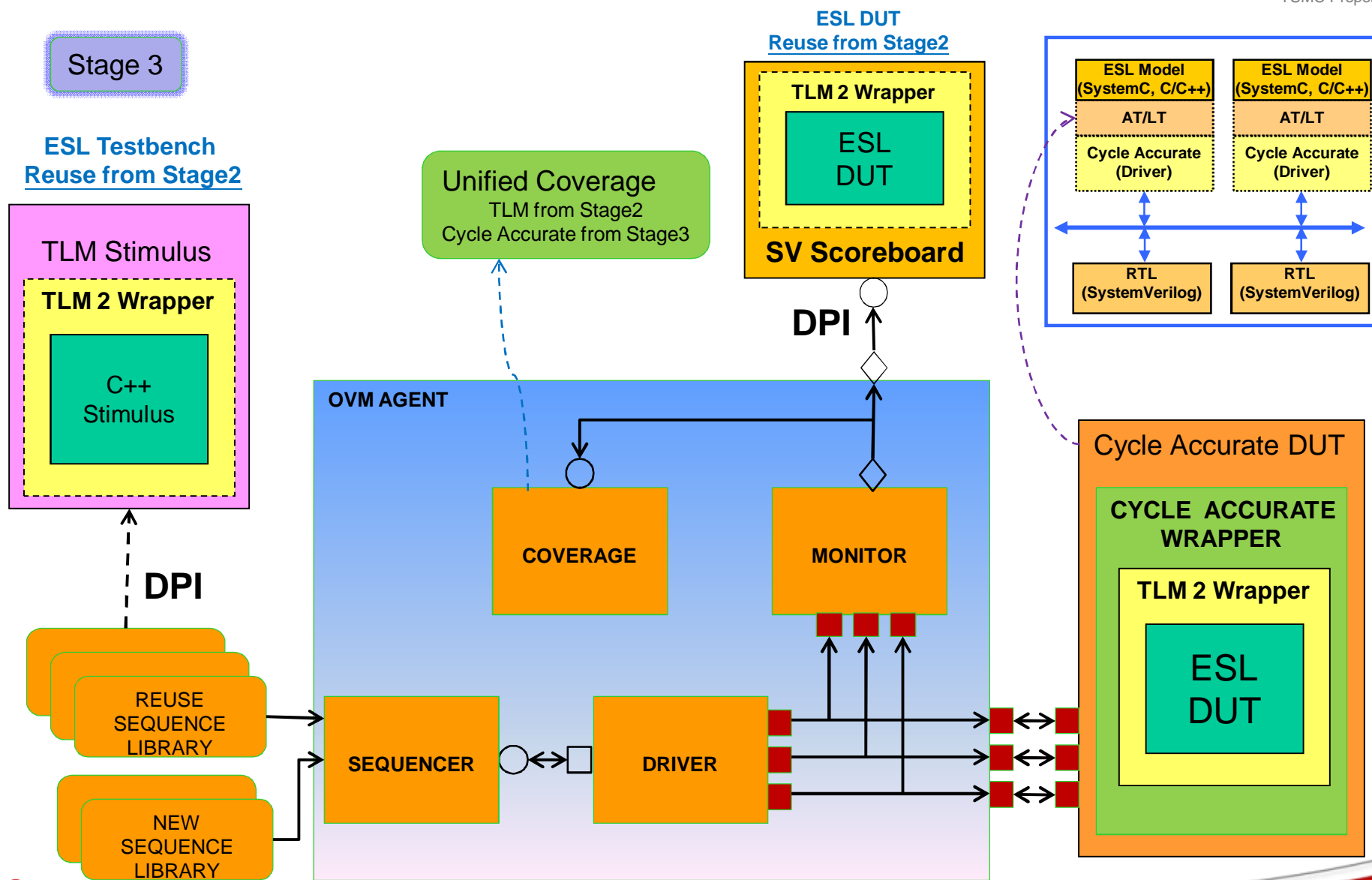
- Verify as much as possible at ESL level. Then
 - Reuse the Testbench, Tests for RTL Verification.
 - Reuse TLM model as a Reference Model for RTL verification
 - Perform stepwise refinement, successively replacing TLM blocks to RTL

- Reuse is not only for the Testbench component but also for the Model component.

ESL Algorithm to TLM Verification Reuse

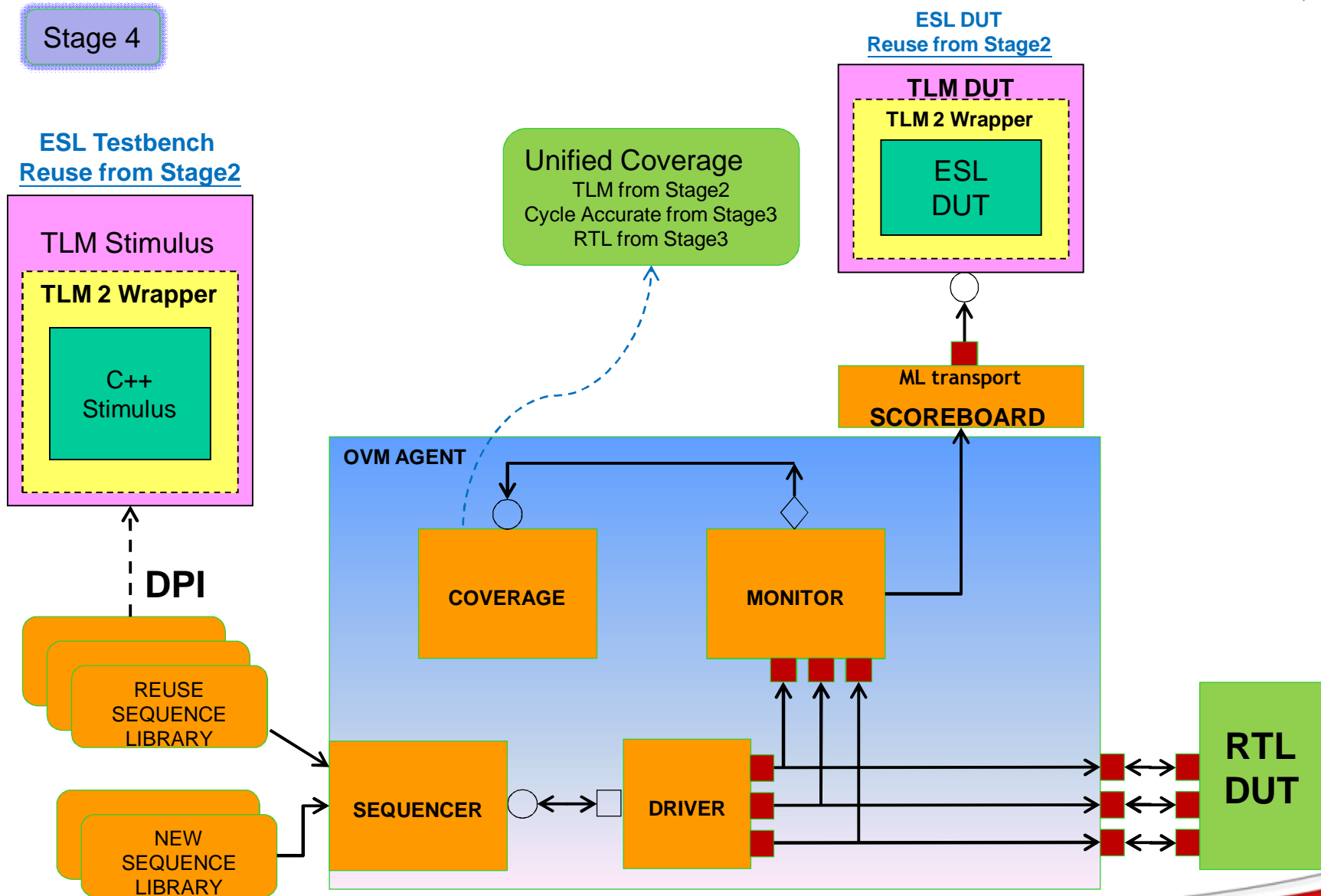


ESL-TLM to ESL-Cycle Accurate Verification Reuse



ESL-TLM to RTL Verification

Stage 4



Summary

- With costs upwards of \$100 million for designs below 40nm, ESL technology will have to become part of mainstream methodology.
- EDA vendors will have to move the entire design and verification ecosystem from RTL to ESL with an easy to use progressively refined reuse methodology.
- OVM is a good candidate to enable ESL Verification

BUT

OVM must support TLM 2.0 – soon



TSMC Property

Thank you ...