



An Innovative Solutions Provider

Successful OVM Deployment



Agenda

- Sibridge Overview
- Benefits of OVM
- VIP Building Imperatives
- Advantages
- Successful Implementation
 - OVM Complaint I2C Verification IP
 - OVM Complaint PCI Express Verification IP



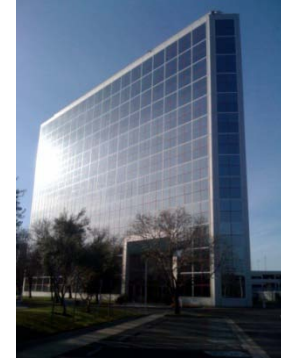
Vision

To partner with leading technology companies and create sustainable value in the product design process by providing IP leveraged solutions



Sibridge Overview

- Electronic Design Services company with spec-to-silicon-to-system experience
- **Expertise**
 - Chip Design & Verification
 - Design & Verification IP development
 - Embedded Software & Product Development
- **Team & Growth**
 - Company growth 40% CAGR
 - 70 + team of technology professionals from premier institutes
 - Team members with multiple success in Silicon Valley
- **Offices**
 - Santa Clara, CA
 - Ahmedabad, India



Santa Clara Office



Ahmedabad Office



Sibridge Team

- **Rajesh Shah, CEO**

- Serial entrepreneur in semiconductor industry with multiple successes
- Sun, PipeLinks (Cisco), Photuris (Meriton), Xpedite (Multilink), Open Silicon (Unicorn PE)



- **Samir Shroff, V.P. Engineering**

- Strong customer solution orientation with perfect blend of semi products and services background
- National, LSI Logic, Silicon Spice (Broadcom), eInfochips



- **Dhruvsh Patel, Director Embedded Systems**

- 15+ years of experience in L2 / L3, High speed 10G, Wireless & N/w
- Experience in Intel, NetEffect, AMCC, Ixia, Texas Instruments, eInfochips, Empirix



- **Shail Talati, Director Business Development**

- 10+ years of experience in Embedded solutions and software space
- HP, Socket, Symbol, HCL



Sibridge Solutions in a Nutshell

- **ASIC & ASSPs**
 - IP selection and Integration
 - Design, Verification and Analog IP provider
 - Digital design & Verification services
 - Migration
 - FPGA based prototypes and emulation
- **Embedded Software**
 - Pre & post silicon firmware development & validation
 - Board support package & RTOS porting
 - Porting & optimization of middleware components
 - Codecs, stacks, algorithms
 - Test Automation Framework development
 - Product design services – board design & software dev



VIP building Imperatives

- Integration/Customization of VIP to perform complete System Level Verification
- Reusability of VIP (from block to chip or to system level verification)
- Ability to verify simultaneously multiple protocols
- Reporting Mechanism status of Verification completeness
- Industry standard language



Without alignment on communication methods and building-block classes, the effort to use VIP can be so large that it is easier to develop verification components from scratch.



Key Benefits of OVM

- **Open**
 - Written in IEEE 1800 SystemVerilog
 - Runs on any simulator supporting the IEEE 1800 standard
 - Verified on Mentor Graphics' Questa and Cadence's Incisive Verification Platform
 - True open-source license agreement (Apache 2.0)
- **Interoperable**
 - Ensures VIP interoperability across ecosystem & simulators
 - Enables VIP 'plug and play' functionality for designers
 - Ensures interoperability with other high level languages
- **Proven**
 - Based on Cadence's Incisive Plan-to-Closure Methodology - URM Component and Mentor's Advanced Verification Methodology (AVM)
 - Incorporates Best Practices from >10 years of experiences



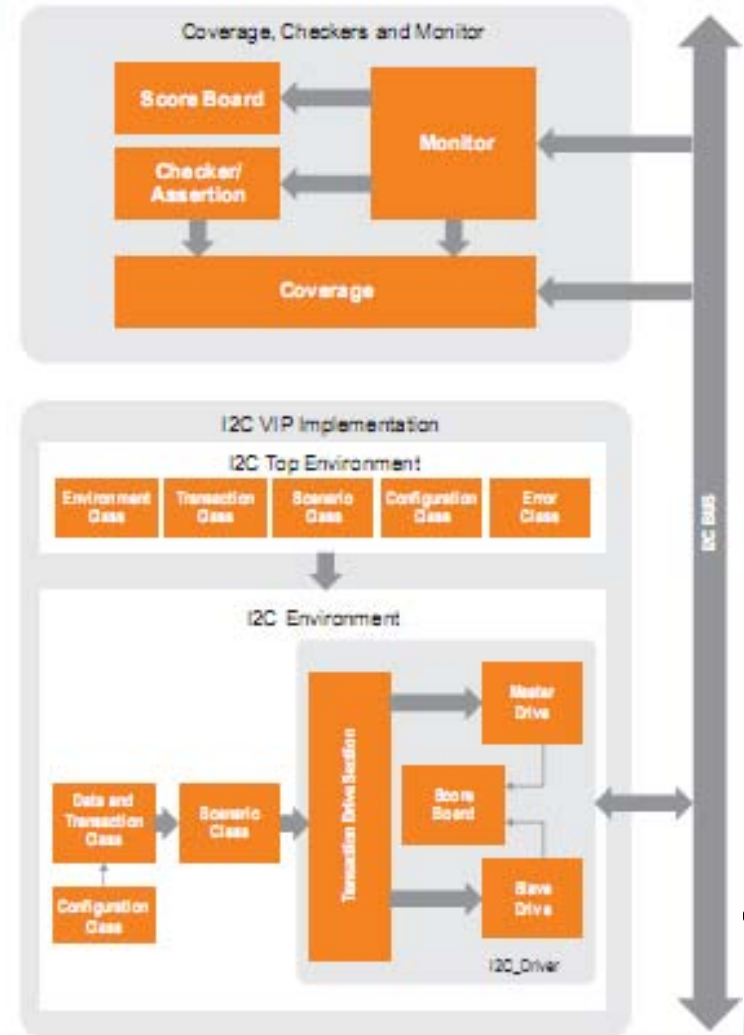
OVM Expertise

- Growing team with 25+ member technical team on OVM know-how
- OVM compliant Verification IP Portfolio
 - I2C Verification IP
 - PCI Express Verification IP
 - Ethernet Verification IP
 - USB under development
 - AXI/AHB/APB under development
- System level verification using OVM based environment
 - Multiple chips taped out with OVM based verification environment
 - Environment with multiple OVM based Verification IPs.



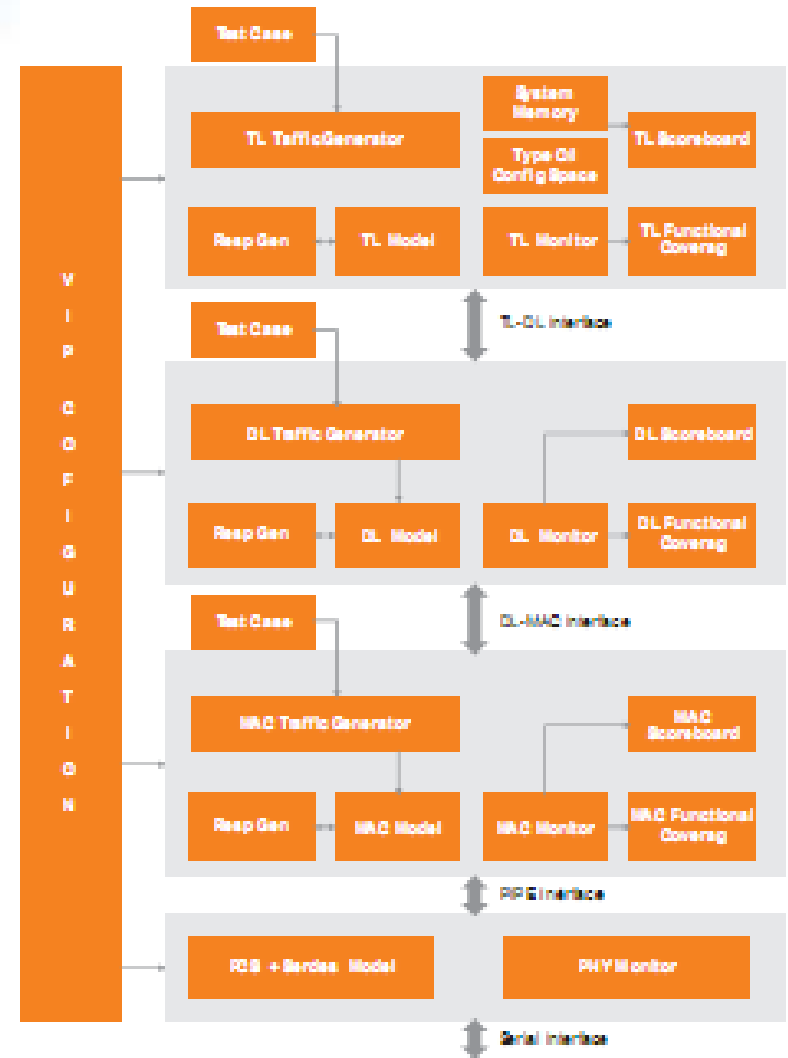
OVM Complaint I2C VIP

- Fully compliant OVM
- Supports directed, constrained random and fully random testing mode.
- Full support for generation of all kind of master and slave errors
- Monitors and checkers for protocol violations
- Coverage model for functional coverage
- Compliant with Questa and Incisive simulators



OVM Complaint PCI Express VIP

- Fully compliant with OVM
- Supports directed, constrained random and fully random testing mode.
- Monitors and checkers for protocol violations
- Coverage model for functional coverage
- In-built scoreboard for data checking at all layers
- Callbacks at each stage of data flow to allow user to modify data flow and transactions on-the-fly
- Compliant with Questa and Incisive Simulators



Thanks

For More Information Visit

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