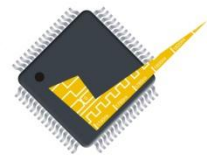




Let's leverage

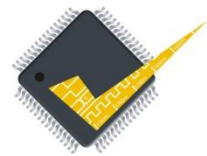
The World's largest Verification IP portfolio  
to Accelerate your designs

## **SuperSpeed your USB 3.0 Verification with OVM based nSys Verification IP**



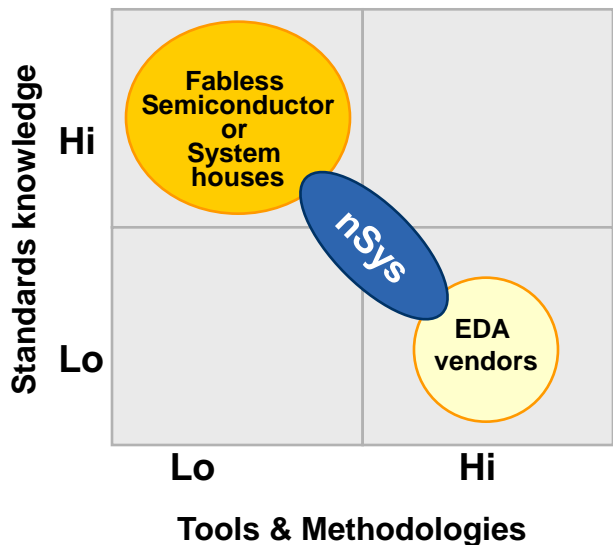
# Outline

- Introduction
- SuperSpeed USB nVS
- Key Features
- Interfaces Supported
- Monitor and Checker
- Coverage
- Bug Details
- nSys' commitment to OVM

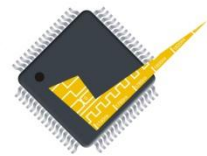


# Introduction

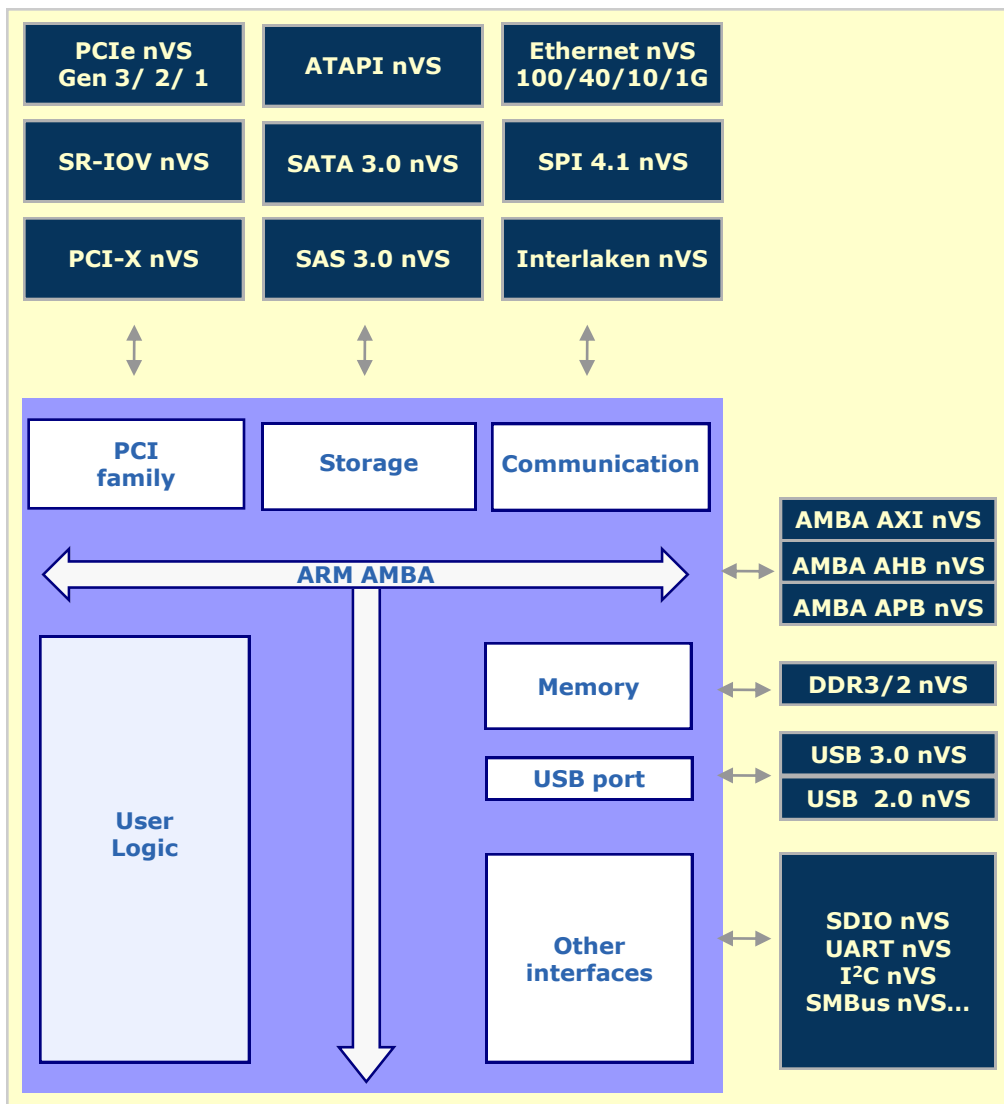
- Largest company with sole focus on Verification IPs & services leveraging them
- Products & Services based upon specialized knowledge of I/O standards & tools
- Observer of multiple Standard Working Groups viz. PCIe protocol, SAS, Accellera etc.



**OVM based Verification IPs to accelerate designs while lowering risks**



# OVM Enabled VIPs: nVS Family



## Defined

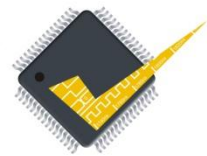
- adj: 'en-vE-&s, feeling or showing envy
- Acronym: **n**Sys **V**erification **S**uite

## Features

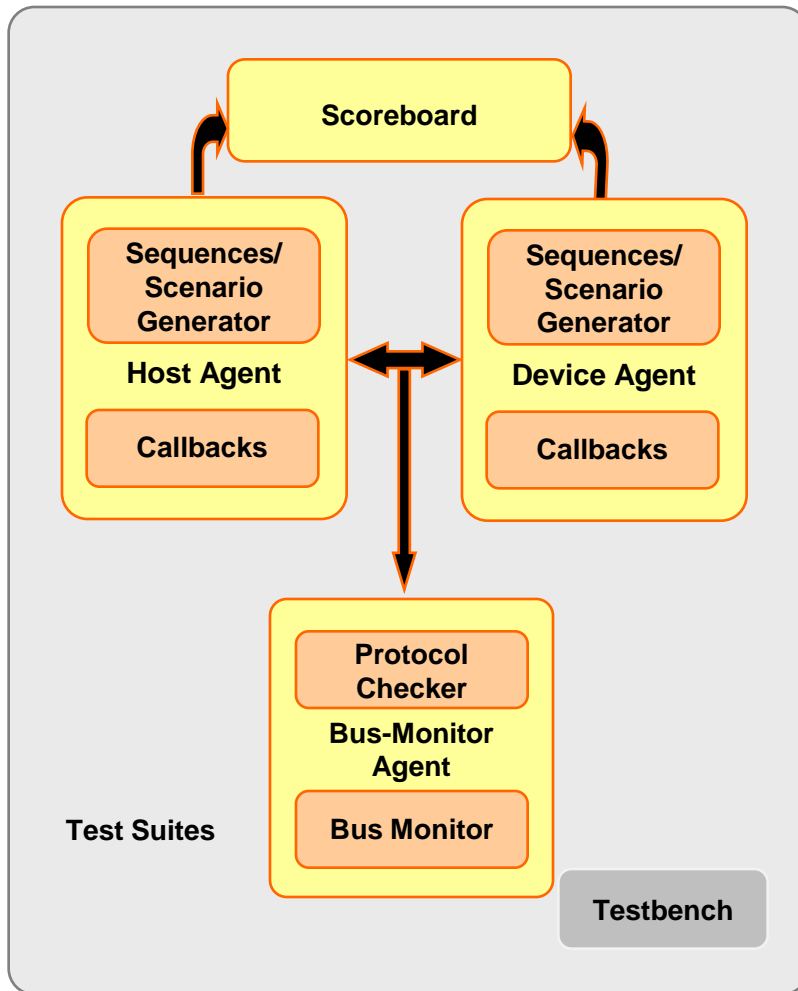
- Extensive Error injection capabilities
- Extensive Coverage
- Standard APIs

## Deliverables

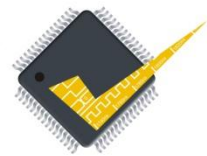
- Validated nVS consisting of BFM, Monitor & Checker as encrypted/ source code
- Test Suites in source code
  - Basic, Error, Random, Directed, Compliance



# SuperSpeed USB nVS

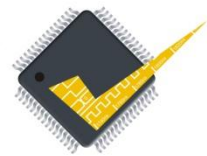


- Compliant to USB 3.0 and USB rev 2.0 Specifications
- Available in SystemVerilog and Verilog
- Consistency of interface, operation, and documentation across nVS family
- Support for all types of USB devices:
  - ✓ Host, Device, OTG, and HUB
- USB 2.0 Support for High, Full, and Low Speed modes
- Support Error Handling
- Capable of extensive error insertion



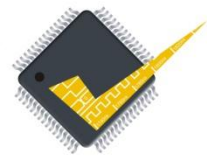
# Key Features ...

- Physical Layer
  - ✓ Support for Symbol Encoding, Symbol Lock, and Scrambling
  - ✓ Support to enable/disable Data Scrambling
  - ✓ Support LFPS transmission/reception
- Link Layer
  - ✓ Configurable entry and exit to/from the Link states
  - ✓ Configurable State Transition timeouts
  - ✓ Configurable counts for receiving/sending
    - TS1/TS2/TSEQ Ordered Sets
    - Logical Idle and LFPS Symbol
  - ✓ Support for low power states: U1, U2, and U3
  - ✓ Supports all Link Commands(LGOOD\_n, LGO\_Un, and LCRD\_x..)



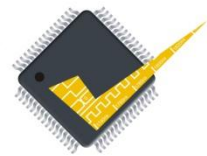
# Key Features ...

- Protocol Layer
  - ✓ Supports Control, Bulk, Bulk Streaming, Interrupt, and Isochronous transfers
  - ✓ Supports multiple Device Configurations and Configurable Endpoints
  - ✓ Supports configurable packet/transaction retries
  - ✓ Supports configurable packets in a burst and configurable burst size
  - ✓ Configurable standard request fields and device response
  - ✓ Configurable device response to Transaction Packet (TP) and Data Packet (DP)
  - ✓ Supports Device Notification Packet, Isochronous Timestamp Packet (ITP), and Link Management Packet (LMP)



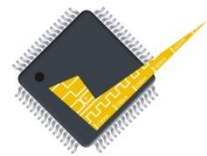
# Interfaces Supported

- Physical Interface:
  - ✓ 1-bit Serial/Differential Interface
  - ✓ 10-bit Parallel Interface
  - ✓ PIPE Interface 8/16/32 bits
  
- SystemVerilog (OVM)
  - ✓ Transaction Class
  - ✓ Callbacks
  - ✓ Sequences



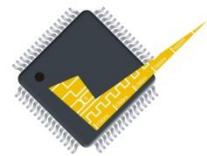
# User Interface: Callbacks

- Callbacks
  - ✓ Transaction received from sequencer
  - ✓ Before calculation of CRC
  - ✓ After calculation of CRC
  - ✓ Before passing to the LL Layer
  - ✓ Before Passing to the PHY Layer



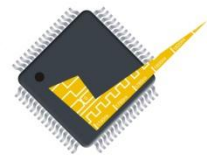
# Coverage

- Coverpoints to track the traffic flow in both directions
- Extensive coverage bins
  - ✓ Transfer Type
  - ✓ Packets
  - ✓ Commands
  - ✓ State Transitions
  - ✓ Functional Checkpoints



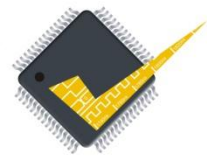
# SuperSpeed your USB 3.0

- Leverage our experience and depth of knowledge in verifying SuperSpeed designs
- Error Prone Areas
  - Link Layer
    - Incorrect LTSSM state transitions
    - Flow Control
  - Protocol Layer
    - Bulk streaming protocol
    - ERDY- NRDY flow control
    - Flow control with ACK having Nump=0
  - Physical Layer
    - Scrambling/ Descrambling
    - 8b/ 10b Encoding/ Decoding
    - LFPS transmission, Receiver detection



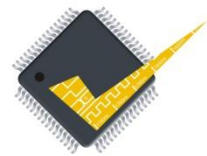
# Bug Details: Link Layer

- TS1 received in between Low Power transition sequence (LGO\_Ux -> LAU -> LPMA)
- LGO\_Ux received in between packet transfer
- Header packet received before header sequence advertisement
- LMP exchange in Hot Reset
- Timeout in Recovery states when Hot Reset attempt is there
- UX\_EXIT\_TIMER violations
- Loopback BERT protocol violations



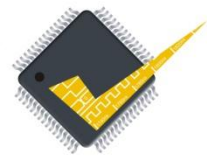
## Bug Details: Protocol Layer

- Behavior on receiving ACK with Nump =0
- Flow control conditions after NRDY/ERDY
- Device response when DPH length is different than DPP length
- Device response when all fields value are not as per specs value
- Nump received in packet is more than Max burst size
- Response to setup packet that come in between control transfer
- Nump > Max burst (Incorrect interpretation of EP companion descriptor, Nump incremented by integer and decremented by 1 )
- Response on receiving DPP > 1024
- Flow control during packet transfer like setup packet, data stage of control transfer and status stage
- Tie-breaker in LMP
- Short packet handling



## Bug Details: Physical Layer

- When to enable/disable scrambling, e.g. DUT's behavior on receiving TS1 in between U0 state
- LFPS transmission in U0 state (Warm Reset)
- Rxvalid low during P0 (PIPE) state
- Effect of SKP ordered sets in counting of TSx ordered sets during Recovery/Polling states
- Assertion/de-assertion of PIPE signals like RxElecdle, TxElecdle during Receiver Detection



## [News > Press Releases : 2008](#)

### **nSys Offers World's Largest Portfolio Of Verification IPs For OVM-based SystemVerilog Environments**

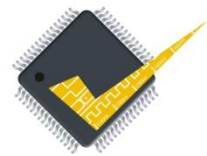
Available for Mentor Graphics Questa Verification Platform

**Newark, CA, Feb 19, 2008:** nSys Design Systems, the developer of the world's largest portfolio of Verification IPs announced today the availability of nSys' Verification IP products integrated with the Open Verification Methodology (OVM) environment. The nSys Verification IPs for OVM-based environments are available for standard interfaces such as AMBA AXI, Ethernet, PCIe, SATA, and USB etc.

"We have seen rapid acceptance of SystemVerilog in the last few months," said Atul Bhatia, CEO of nSys Design Systems. "The availability of commercial verification tools from nSys and Mentor Graphics will help mutual customers leverage the full potential of SystemVerilog and OVM to develop verification environments that before were only a dream."

The demand by users for verification data portability and verification platform interoperability has driven the verification community to OVM. Being a member of Mentor Graphics Questa Vanguard program, nSys is able to qualify its Verification IP with the Questa verification platform and offer early support for OVM. As a recognized OVM Partner, nSys can leverage electronic design automation industry collaboration in the development and support of OVM as well as provide early feedback and rapid support of OVM.

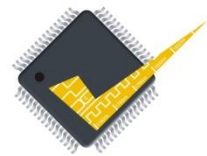
"We worked closely with nSys upon the release of OVM so our mutual customers could use the nSys Verification IPs within the Questa verification environment," said Dennis Brophy, Director of Strategic Business Development of Mentor Graphics Design Verification and Test division. "The availability of nSys Verification IPs for OVM-based environments will enable designers to rapidly adopt OVM and drastically reduce the verification effort of complex designs."



# nSys' Commitment to OVM



- nSys is a part of Mentor's Questa Vanguard program for building a strong and comprehensive SystemVerilog ecosystem.
- World's largest portfolio of Verification IPs in native SystemVerilog & Verilog
- All the Verification IPs from nSys are OVM Enabled



# Thanks



Accelerating designs

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