

Verification Productivity

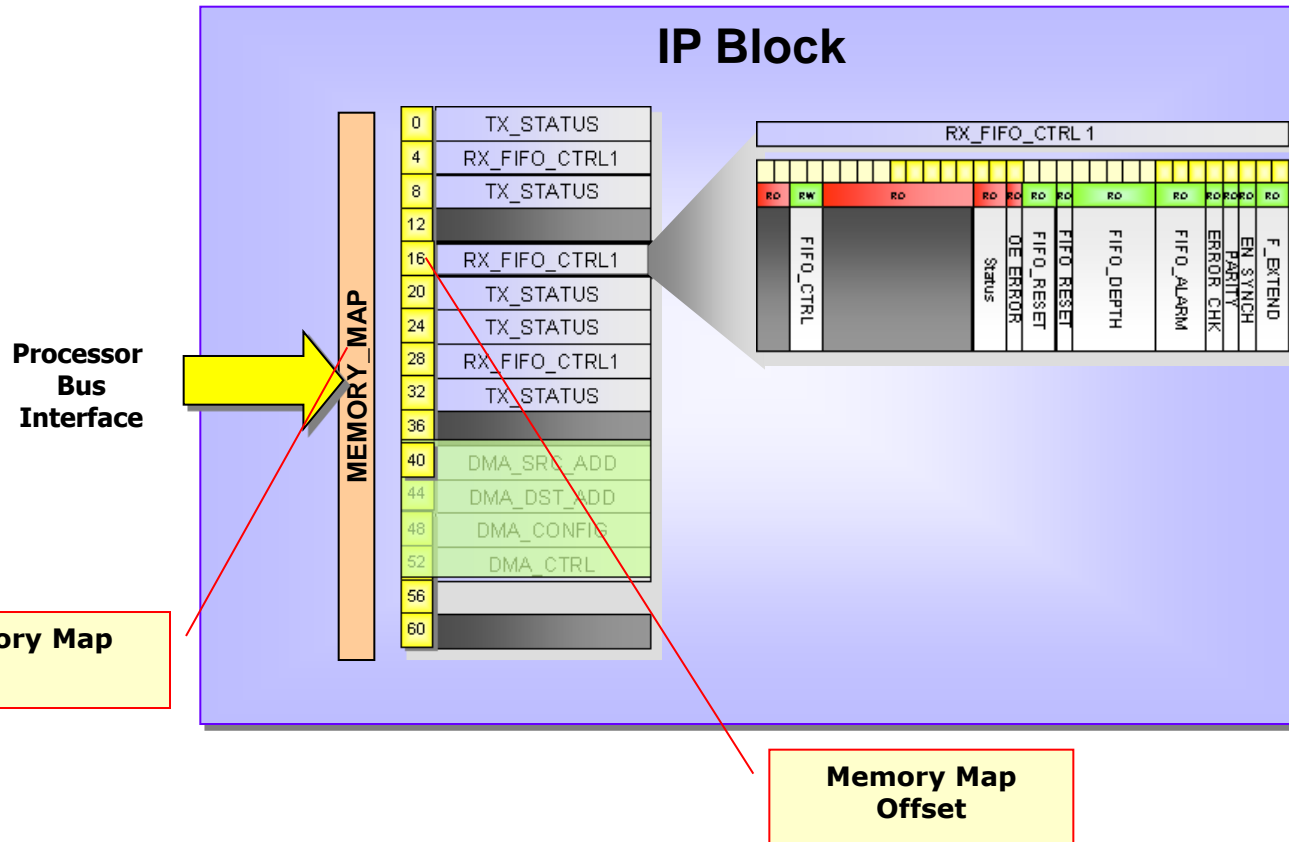
Introducing and Eliminating the GNAT



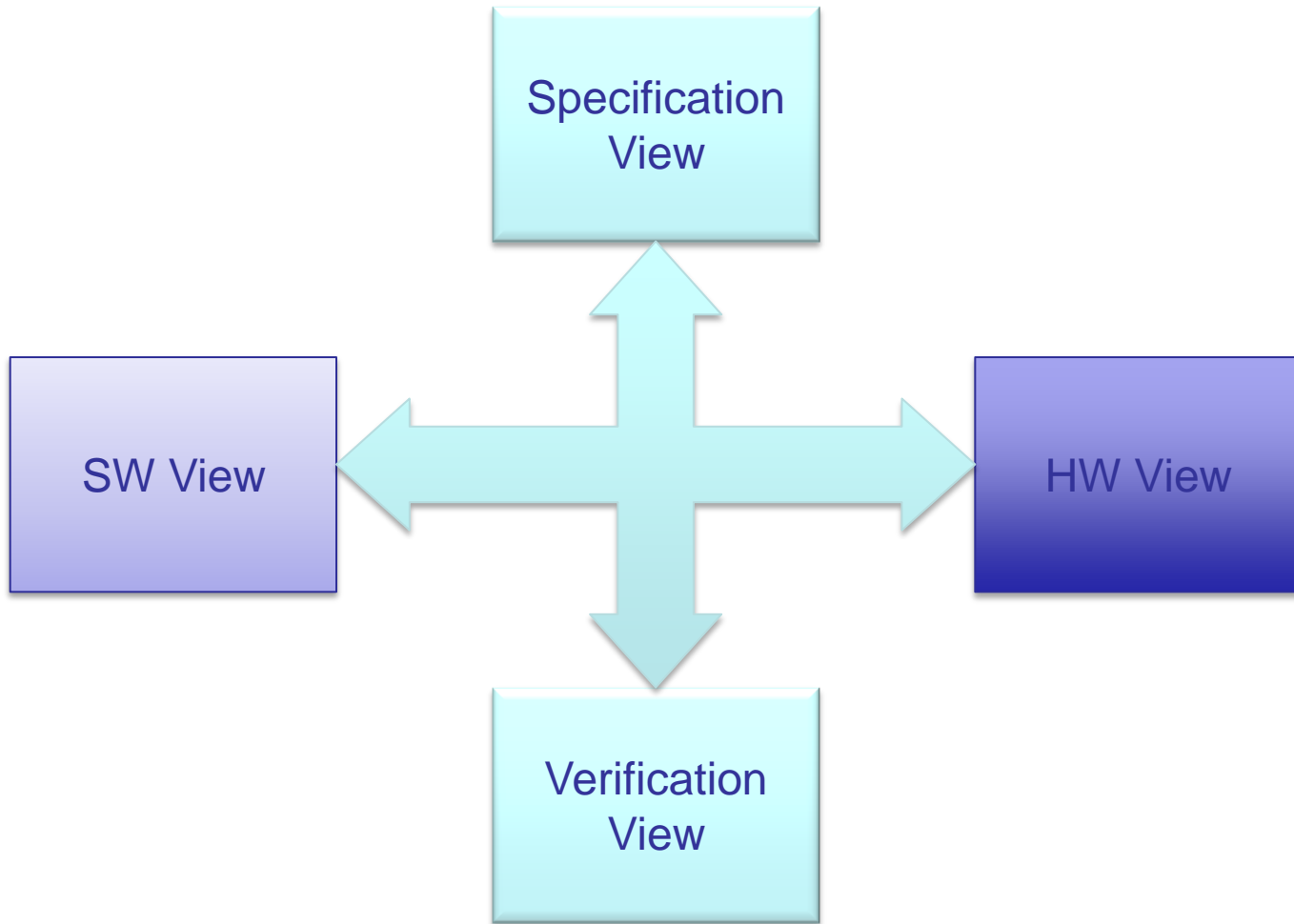
David Murray
CTO
Duolog Technologies



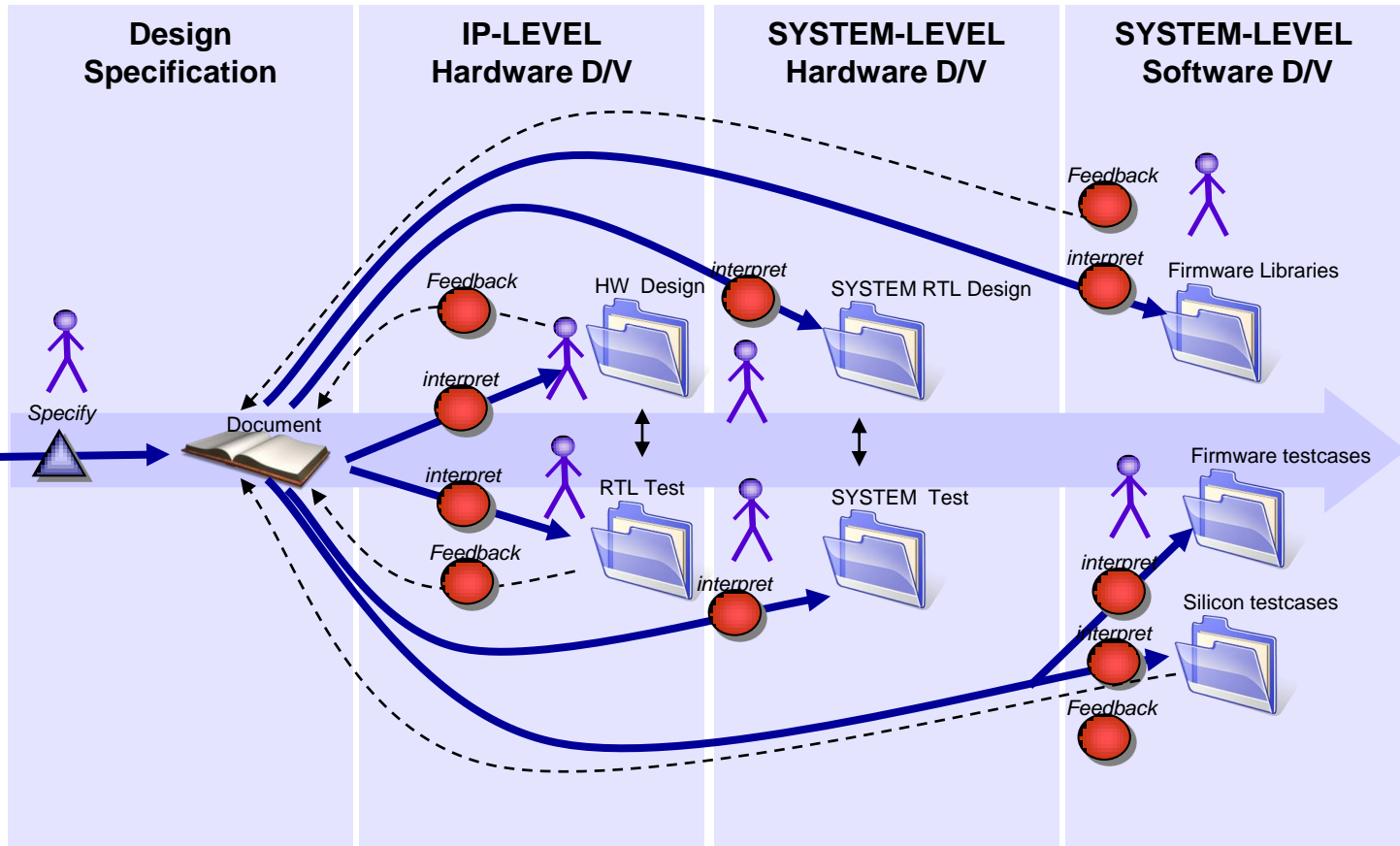
HW/SW Interface (SW View)



HW/SW Interface (Verification)

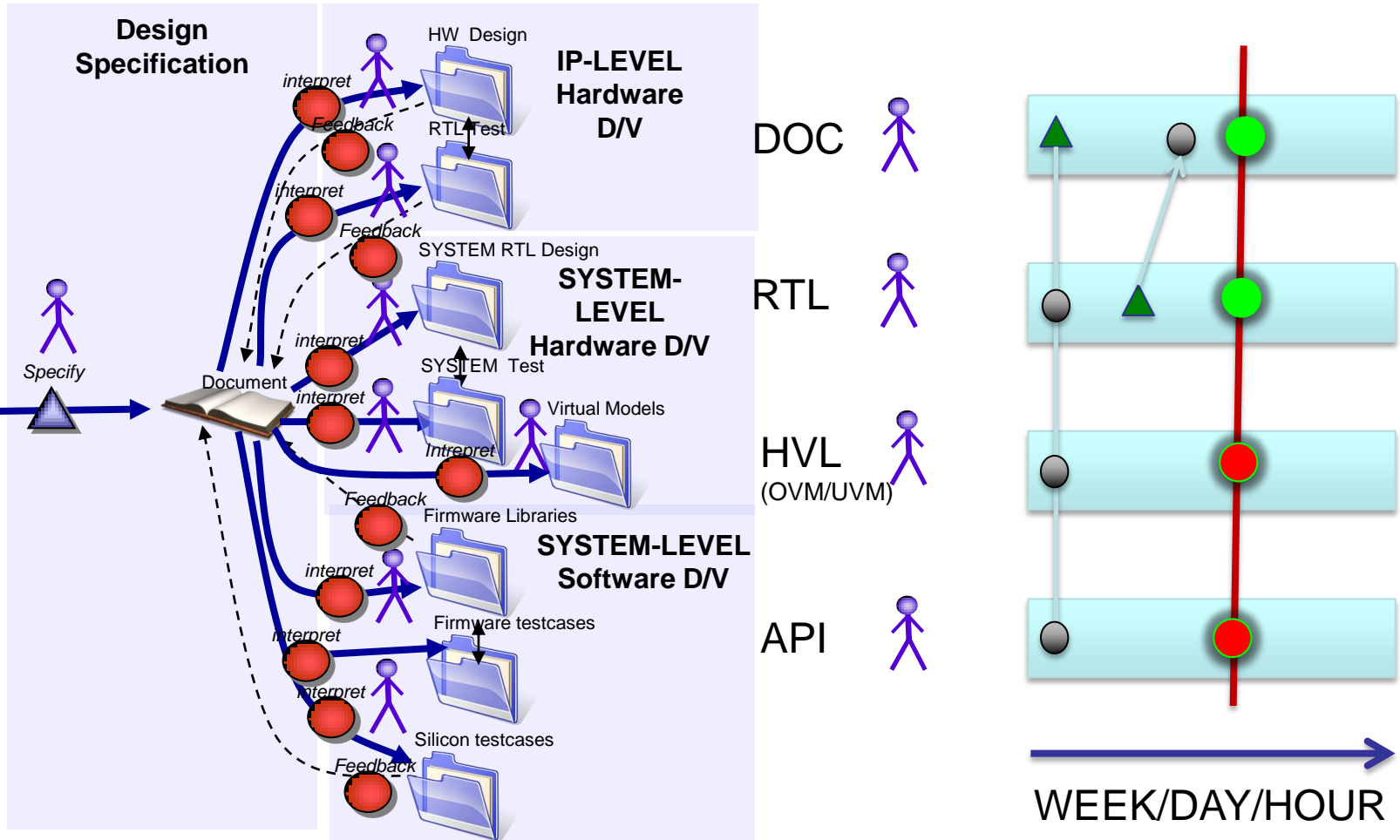


Traditional HW/SW Interface



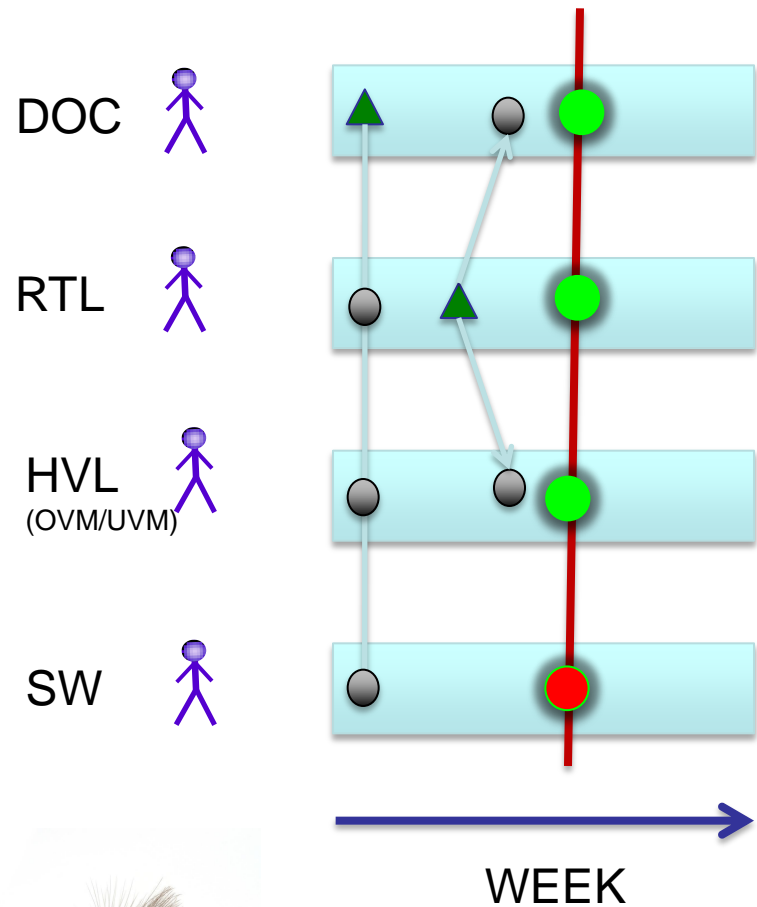
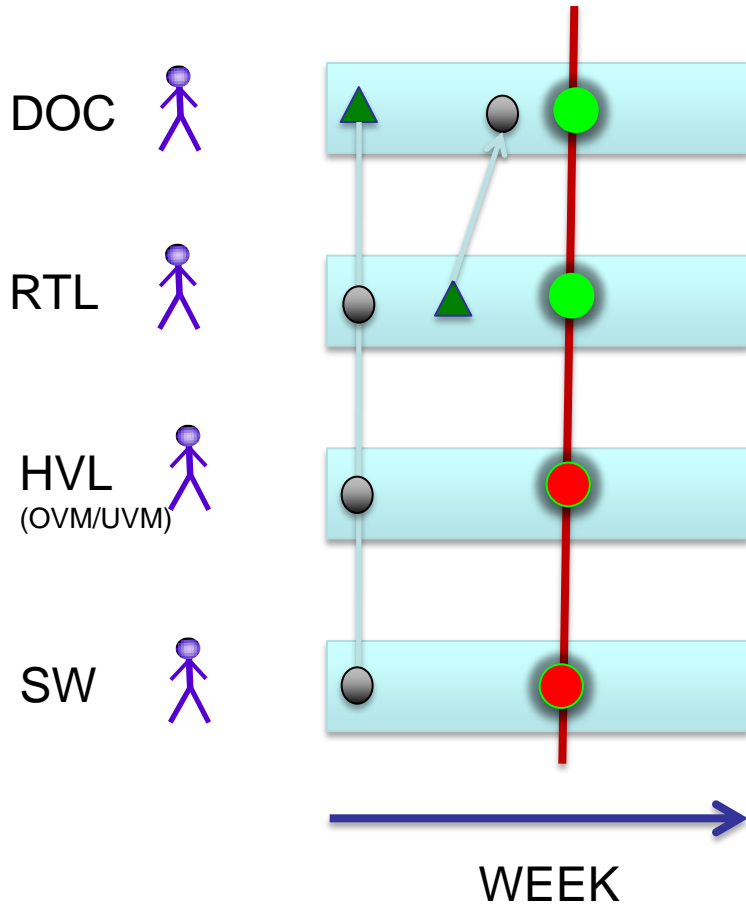
Refinement points/Milestones

Compressed Design Cycle





Misalignment





DOCUMENT DRIVEN

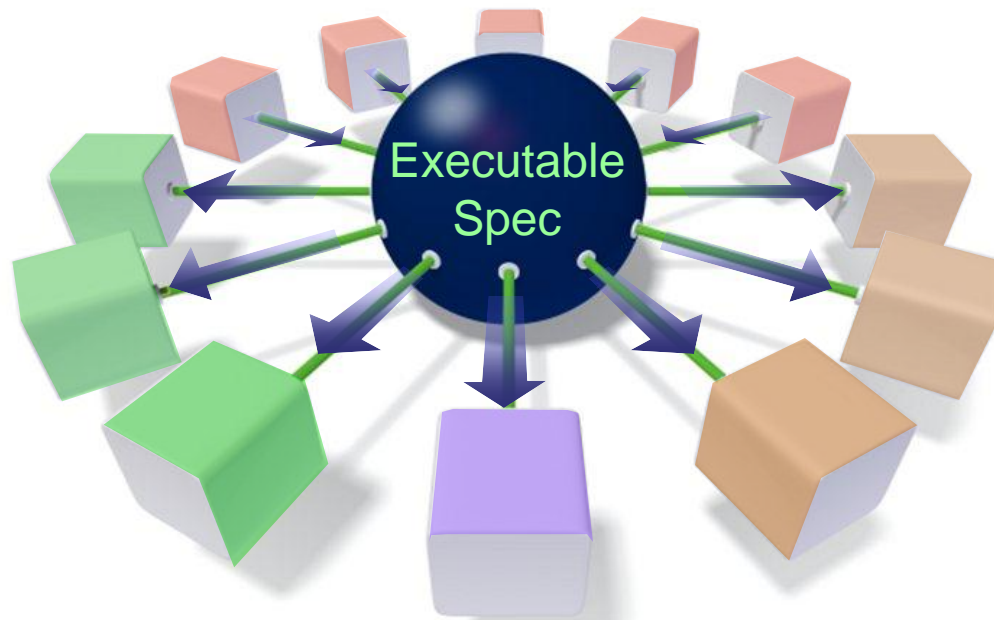


Executable Specification

CAPTURE

HW Interface : interfaces & psorts

SW Interface : registers, memories, memory maps



VALIDATE

Correct Data
Coherent specification

GENERATE

Design source

HW/SW ⇔ Design/Verification ⇔ Specification/Implementation



Socrates Chip Integration Hub



Standardize ↔ Centralize ↔ Synchronize

IP packaging and standardization
IP integration/Chip assembly
I/O integration

Port-to-Pin
HW/SW views

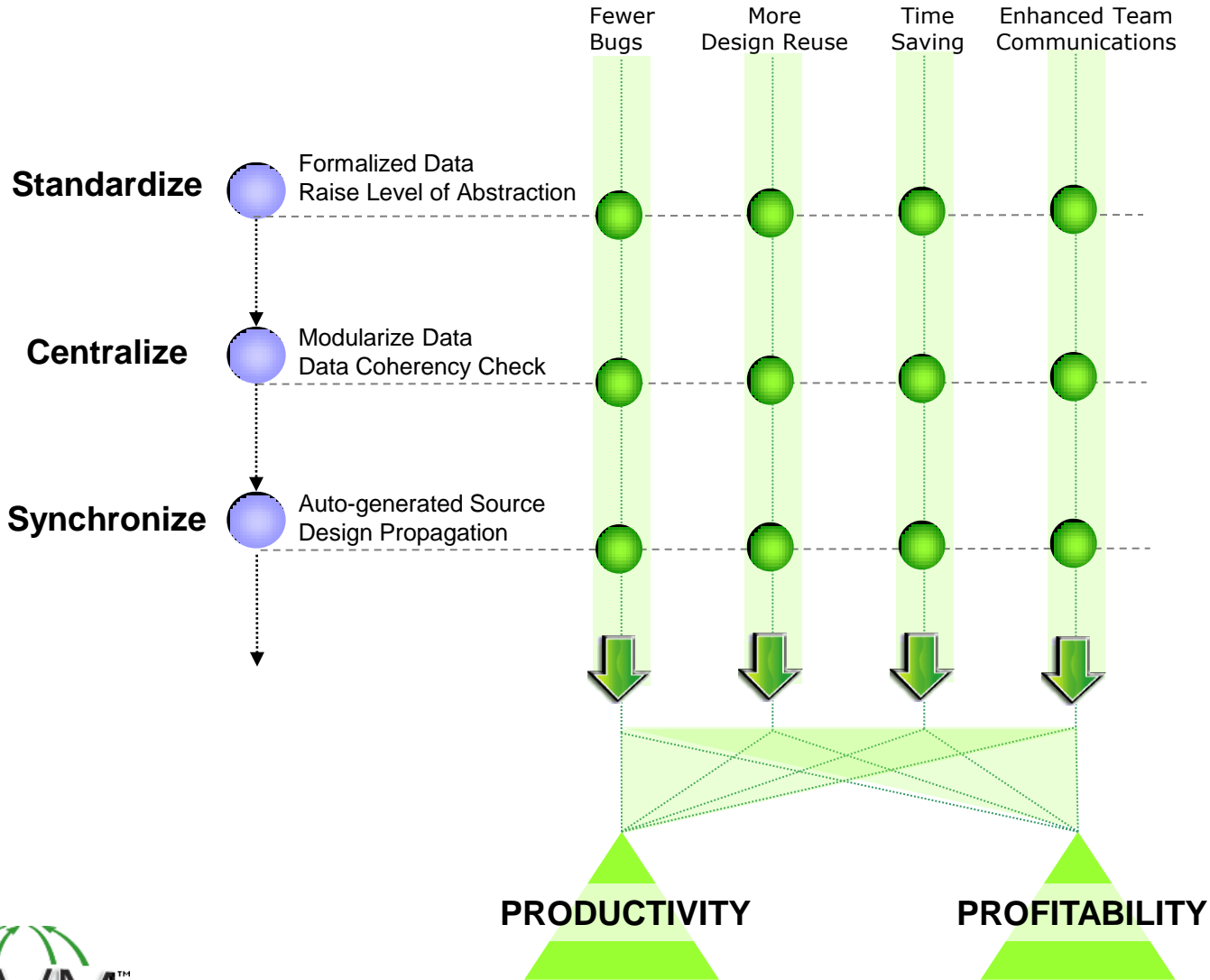
Generated Design Views

Teams Views		Teams						Software
		Architecture	HW Design	Module Verification	System Integration	System Verification	Synthesis/Backend	
Documentation	Integration Specification	✓	✓	✓	✓	✓	✓	✓
	Verification Plan			✓		✓		✓
	Programmer's Guide	✓		✓		✓		✓
	Review docs	✓	✓	✓	✓	✓	✓	✓
RTL	Structural RTL	✓	✓		✓	✓	✓	
	Functional RTL		✓	✓	✓	✓	✓	✓
	Behavioural RTL	✓		✓		✓		
HVL	Specman VR_AD			✓		✓		
	'e' Test Cases			✓		✓		
	VMM RAL Description			✓		✓		
	OVM/UVM SystemVerilog			✓		✓		
Software	SystemC PV	✓				✓		✓
	C API/HAL	✓				✓		✓
	C Test Cases					✓		✓
	Custom Views	✓	✓	✓	✓	✓	✓	✓
	Total Views Needed	✓	✓	✓	✓	✓	✓	✓





Benefits





THANK YOU!